**Project on UART**

Made by :-

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A **universal asynchronous receiver transmitter** (**UART**) is a [computer hardware](https://en.wikipedia.org/wiki/Computer_hardware) device for [asynchronous serial communication](https://en.wikipedia.org/wiki/Asynchronous_serial_communication) in which the data format and transmission speeds are configurable. The electric signaling levels and methods are handled by a driver circuit external to the UART. A UART is usually an individual (or part of an) [integrated circuit](https://en.wikipedia.org/wiki/Integrated_circuit) (IC) used for [serial communications](https://en.wikipedia.org/wiki/Serial_communications) over a computer or peripheral device [serial port](https://en.wikipedia.org/wiki/Serial_port). One or more UART peripherals are commonly integrated in [microcontroller](https://en.wikipedia.org/wiki/Microcontroller) chips. A related device, the [universal synchronous and asynchronous receiver-transmitter](https://en.wikipedia.org/wiki/Universal_synchronous_and_asynchronous_receiver-transmitter) (USART) also supports synchronous operation.

In my project I have made three Verilog files, one for Baud rate generator, one for transmitting the data bit by bit and one for the receiver. I have made this project such that the data is being transmitted bit by bit means serially and we get the output in one cycle means parallelly. And after transmitting the data, the transmitter is shut down meaning the “tx” (name of the data type used in transmitter to transmit data bit by bit) is at high impedance indicating that the transmitter is not in working condition. And we get the output after 10 clock cycles, 8 clock cycles for the 8 bit data and the additional 2 bits are for start and stop bit. Here I have used ‘0’ as a start bit and ‘1’ as a stop bit. After giving the output in the 11th clock cycle, the receiver is reset means that all the output and input of receiver are cleared and the output data is set as high impedance indicating that there is no data present and the receiver isn’t in working condition.

INPUT SIGNALS

* ‘ipclock’ – This is a signal of 1 bit which is used for the internal clock . It is used to synchronize the operations of the system . In this project , it has a 50% duty cycle with time period of 40 ms .
* ‘selection’ – This is an input signal of 2 bits used in Baud rate generator module. This is used to set the value of ‘count’ according to the different baud rates.
* ‘datain’ – This is a signal of 8 bit used in transmitter block . It will receive 8 bit data as an input entered by the user.
* ‘readyip’ – This is an input signal of 1 bit which will determine the state of the transmitter block. If the value of readyip is ‘0’ then it means that transmitter block is in off state and isn’t transmitting the data. And the transmitter block will transmit the data if the value of readyip is ‘1’.
* ‘rx’ – This is a signal of 1 bit used in receiver block. This will receive one bit data as an input to the receiver.

OUTPUT SIGNALS

* ‘count’ – This is a integer type output used in Baud-generator module. This will tell the value of UxBrg whose value is given by :-

UxBrg = (freq/(16\*Baud\_rate)) – 1

Its value will change according to the Baud rate.

* ‘tx’ – This is a signal of 1 bit which is an output of reg type in the transmitter module. This is used to transmit data serially (bit by bit). It will be in off state which is high impedance after sending all the bits of the data and will remain in that state until the transmitter is ready.
* ‘readyop’ – This is an output signal of 1 bit which will tell if the data has been transmitted by the receiver.
* ‘data’ – This is a signal of 8 bit and reg type used as an output in the receiver block. This will give the output after 10 clock cycles. And after giving the output , it will reset and will be in the off state, its value will be high impedance.

SIMULATION

